Electrostatic Dimension of Aligned-Array Carbon Nanotube Field-Effect Transistors

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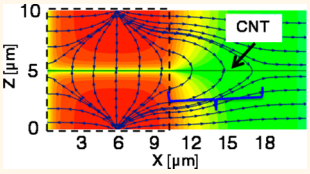
ABSTRACT Accurate electrostatics modeling of nanotubes (NTs)/nanowires (NWs) has significant implications for the ultimate scalability of aligned-array NT/NW field-effect transistors (FETs). The analysis to date has focused on limits of capacitive coupling between the 1D channel and 2D gate that is strictly relevant only in the linear response operation of NT/NW-FETs. Moreover, the techniques of electrostatic doping by independent gates that cover only part of the channel are widely used, but the nature of its electrostatic coupling has not been explored. In this paper, we use a three-dimensional, self-consistent model for NT/NW-FETs to interpret the essence of electrostatic coupling with complex configuration of electrode geometries. The interplay between 3D electric fields and its 1D termination onto the NTs/NWs suggests surprising complexity of electrostatic interaction not captured in simpler models. This coupling can change the performance metrics such as ON and OFF currents by orders of magnitude depending on (1) NT/NW density, (2) bias voltage, and (3) gate overlap length. Remarkably, this parasitic coupling persists regardless of the gate oxide thickness, changes in dielectric constant, and/or the width of the diameter distribution of NTs/NWs. The predictions of the model are systematically validated by a series of experiments.



KEYWORDS: aligned-array carbon nanotubes · tube density · partial-gate transistor · three-dimensional electrostatics · parasitic gate coupling · band-to-band tunneling · high field transport

Emergence of the nanotubes (such as carbon nanotube, boron nitride nanotube, molybdenum disulfide nanotube, and tungsten disulfide nanotube) and nanowires (such as silicon nanowire, III–V, and II–VI compound semiconductor nanowires) has attracted attention of researchers because of their exclusive 1D structure.[1−3] Interest in nanotube (NT)/nanowire (NW) electronics has been sustained by a broad range of potential applications (*e.g.*, digital/analog electronics,[4−8] memory,[9,10] display,[11,12] optoelectronics,[8,13,14] and chemical/biosensing[15,16]) enabled by the unique electrical, optical, chemical, topological, and percolative properties of single, array, and networks of NTs/NWs. The essential building blocks in these applications are field-effect transistors (NT/NW-FETs) in three- or four-terminal configurations.[14,17−21] Electrical (*e.g.*, mobility, conductivity, contact resistance, coefficients of impact ionization, coefficients of band-to-band tunneling), optical (*e.g.*, quantum yield), and sensing (*e.g.*, sensitivity) parameters extracted in these applications depend on the electrostatic interpretation of gate control on NTs/NWs. In the traditional approach, the capacitance between the channel and gate is calculated by using two-electrode geometry (where NTs/NWs form lines[4,22] or thin films[4,22,23] on a plane, or are surrounded by a gate in a coaxial geometry[22]) with appropriate correction for NT/NW density.[23,24] This presumption of 2D symmetry along the channel direction is generally appropriate for interpreting linear response (low V_{DS}) of NT/NW-FET operation, especially with full-gate coverage[4,7,25−29] (Figure 1a). As the drain bias is increased or partial gates (necessary for electrostatic doping[13,14,17,20] and for obtaining better control in conduction for different chiralities[30−32]) are turned on, the 2D symmetry along the channel is

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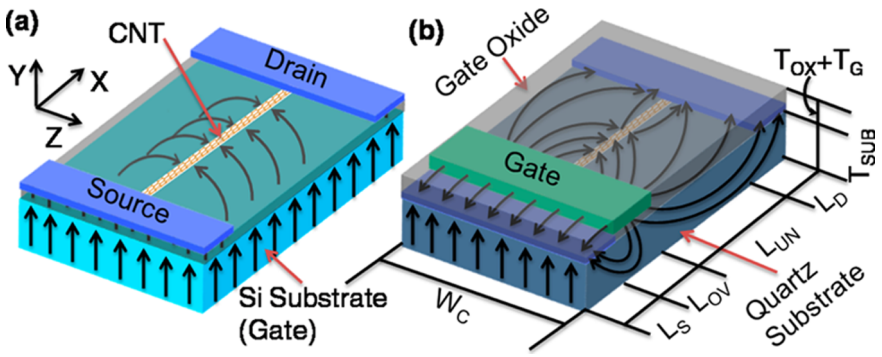

Figure 1. Schematic illustration of the electric field distribution in a (a) full-gate CNTFET (FG-FET) and (b) partial-gate CNTFET (PG-FET), with CNT as the channel. For FG-FET, the gate dictates the electrostatics of CNTs, whereas for PG-FET, the gate controls CNT electrostatics of the entire overlap region (length: L_{OV}) and part of the underlap region (length: L_{UN}) through parasitic coupling. As we show later, the extent of this coupling depends on CNT density (N). Here, $W_C = 1/N$ is the electrostatic width shared by one CNT in an array, $L_{D(S)}$ is the drain (source) length, and T_{SUB}, T_{OX}, and T_G are the thickness of quartz substrate, gate oxide, and gate contact, respectively.

broken, and the 3D field lines from the electrodes terminate onto quasi-1D NT/NW conductors through fringing fields (Figure 1b). As a result, effective electrostatic dimension that apportions the relative control of gate and drain over the channel (and corresponding performance metrics) of these devices evolves with biasing configuration.[33,34]

In this paper, we use a 3D electrostatic simulation of especially designed partial-gate FETs (PG-FETs) with variable single-wall carbon nanotube (CNT) density to explore the implications of three-dimensional electrostatic coupling between electrodes and NT/NW channels. (Although we analyze the carbon nanotubes in this work, the essential physics and conclusions should also be applicable for other 1D nanotube and nanowire transistors.) Our analysis offers an intuitive interpretation of the evolution of the parasitic gate control (through fringing fields) as a function of biasing configuration, CNT density, and finite size of the electrodes. Irrespective of the gate oxide thickness, dielectric constant, and CNT diameter, our theoretical results show the following: (1) The effect of 3D coupling is most significant for single-tube or low-density arrays (relevant for most experiments published in CNTFET literature), and as a result, the performance metrics such as ON and OFF currents may differ by orders of magnitude from those predicted by traditional 2D electrostatic model. (2) Although parasitic gate−CNT coupling is suppressed with increasing CNT density, the residual coupling is still significant, and therefore, unless the density approaches the charge-sheet limit (>100 CNTs/μm), the OFF state tunneling current cannot be predicted by a 2D model, even for moderately high densities. (3) Device parameters such as mobility, tunneling coefficients, *etc.*, extracted by 2D interpretation of these devices, are likely to be incorrect. Finally, (4) the 2D limit is only approached asymptotically for very high tube density (N > 100 CNTs/μm).

The paper is organized as follows. In the following section, we use a self-consistent simulation framework that couples the 3D Poisson equation with the 1D drift-diffusion transport.[35] The drift-diffusion model has been generalized to include tunneling and impact ionization phenomena and carefully calibrated to 1D transport in CNTs. This model is then applied to predict the characteristics of partial-gate FET (PG-FET) as a function of tube density (N), gate overlap length (L_{OV}), and drain bias (V_{DS}). We find that the complex electrostatic interaction in a PG-FET results in significant and somewhat counterintuitive variation in ON and OFF currents as a function of device parameters. Theoretical predictions are later validated against a series of experiments. The universality of the model is observed by analyzing the effects of gate oxide thickness (T_{OX}), dielectric constant (ε_{OX}), and CNT diameter (d). We conclude the paper with a summary of the analysis and a few comments regarding the generality of our conclusions.

RESULTS AND DISCUSSION

PG-FET Modeling and Simulation Results. The extent of deviation from classical 2D electrostatics and quasi-3D gate control on the electrostatics of PG-FET are simulated by varying $N \sim 1/W_C$ of aligned-array CNTs (Figure 1b), where W_C is the spacing between the CNTs in an array. CNTs with diameter d = 1.74 nm are spaced uniformly with pitch W_C. Self-consistent solution of the Poisson and drift-diffusion equations[35] with appropriate device geometry simulates the band profile and currents in PG-FET. Solution of the three-dimensional Poisson equation captures the effect of contact dimensions, and the drift-diffusion equation describes one-dimensional carrier transport along the CNT. Analytical expressions for field-dependent mobility[25,35,36] and carrier densities are calibrated from independent experiments,[37−39] and CNTs are doped with acceptors to capture the influence of (oxygen- and water-induced) negatively charged interface defects.[40,41] We also use extensively and independently calibrated models for

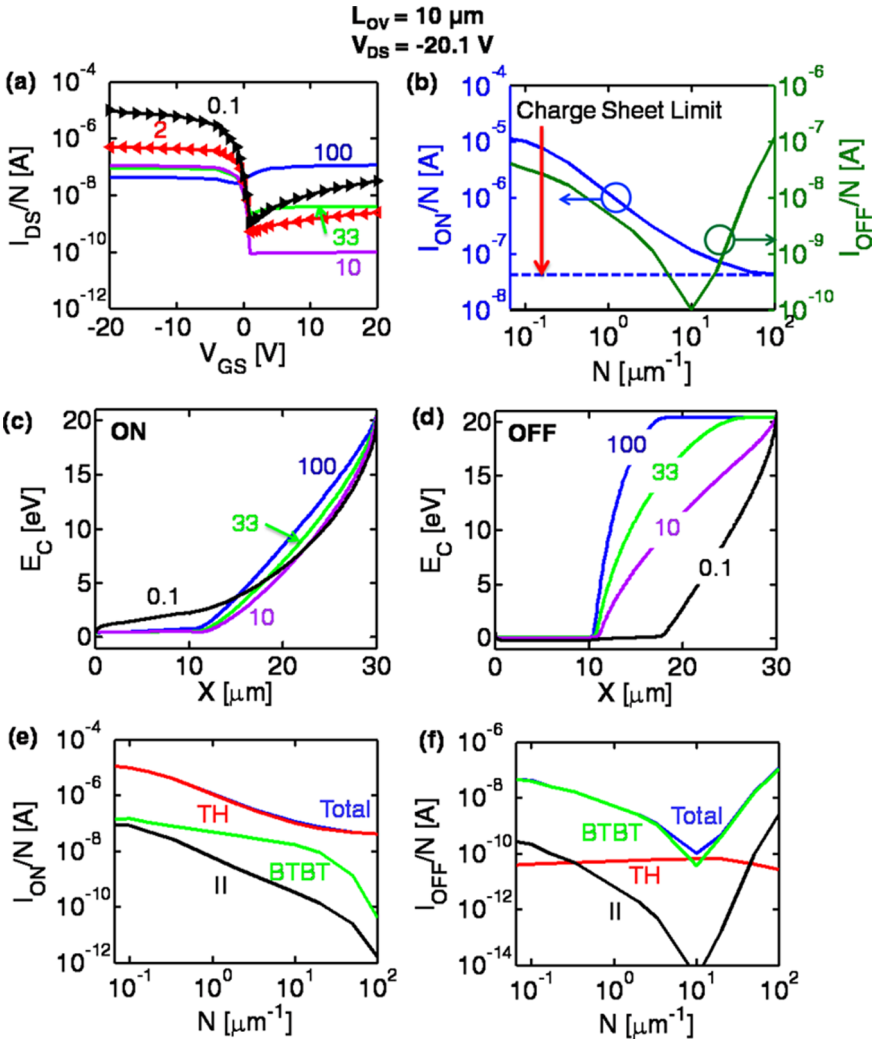

Figure 2. (a) $I_{DS}-V_{GS}$ characteristics of PG-FET suggest strong dependence on *N*. (b) Plot of I_{DS} per CNT from such characteristics at $V_{GS} = -20$ V (I_{ON}/N) and $V_{GS} = 20$ V (I_{OFF}/N) as a function of *N*. A unique feature of V-shaped I_{OFF}/N *vs N* relationship is only expected from 3D electrostatic simulation of PG-FET. A dotted line drawn is the I_{ON}/N at charge-sheet limit (maximum attainable CNT density: ~574 CNTs of diameter 1.74 nm in 1 μm width) condition. (c,d) Conduction band profiles for different *N* in ON and OFF states. (e) I_{ON}/N for any *N* is dominated by the thermionic injection of carriers (TH) over the hole-energy barrier near the source contact and subsequent drift of hole through CNTs. (f) In OFF state, BTBT is the dominant current component. The schematic band diagrams are shown in Supporting Information Figure 1a,b corresponding to low-density and high-density CNTs in order to explain different leakage current components in the OFF state.

the probability of band-to-band tunneling[17,20,42] (BTBT) and impact ionization[42] (II) at location *x* along the CNT using $\sim \exp[-E_{C,BTBT(II)}/(dV/dx)]$,[42] where $|dV/dx|$ is the electric field along the channel direction and $E_{C,BTBT(II)} \sim 1/d^2$ is the critical field for BTBT (II). See Methods section for modeling details.

Figure 2a shows drain current (I_{DS}) *versus* gate voltage (V_{GS}) characteristics of a PG-FET for a broad range of $N \sim 0.067-100$ CNTs/μm (with $L_{OV} = 10$ μm, channel length $L = L_{OV} + L_{UN} = 30$ μm, $L_{S/D} = 2$ μm, oxide thickness $T_{OX} = 400$ nm, source/drain contact thickness $T_{S/D} = 40$ nm, gate contact thickness $T_G = 200$ nm, and substrate thickness, $T_{SUB} = 6$ μm) operated at high source–drain bias, $V_{DS} = -20.1$ V. The $I-V$ characteristics at all densities show features of ambipolar transport. The decrease of ON current (*i.e.*, I_{DS} at $V_{GS} = -20$ V) per CNT (I_{ON}/N) in Figure 2b is expected using the classical drain current and oxide capacitance expressions of $I_{DS} \sim C_{OX}(V_{GS} - V_T)V_{DS}$ and $C_{OX} = 2\pi\varepsilon_0\varepsilon_{OX}N/\ln[\sinh(\pi(2T_{OX} + d/2)N)/\sinh(\pi dN/2)]$,[4,23,43] where ε_0 is the free space permittivity and ε_{OX} is the dielectric constant of the gate oxide. Analytically calculated I_{DS}/N follows simulation (not shown), with differences that can be attributed to the full-gate and partial-gate geometries used for analytical and simulation approaches, respectively. To calculate the highest density (*i.e.*, charge sheet) limit of ON current, let us consider a tightly packed array with CNT spacing equal to the diameter of the tube (~1.74 nm), with corresponding density of ~574 CNTs/μm. We simulate the device for this CNT density and find that, in this highest density limit, the ON state current per CNT is

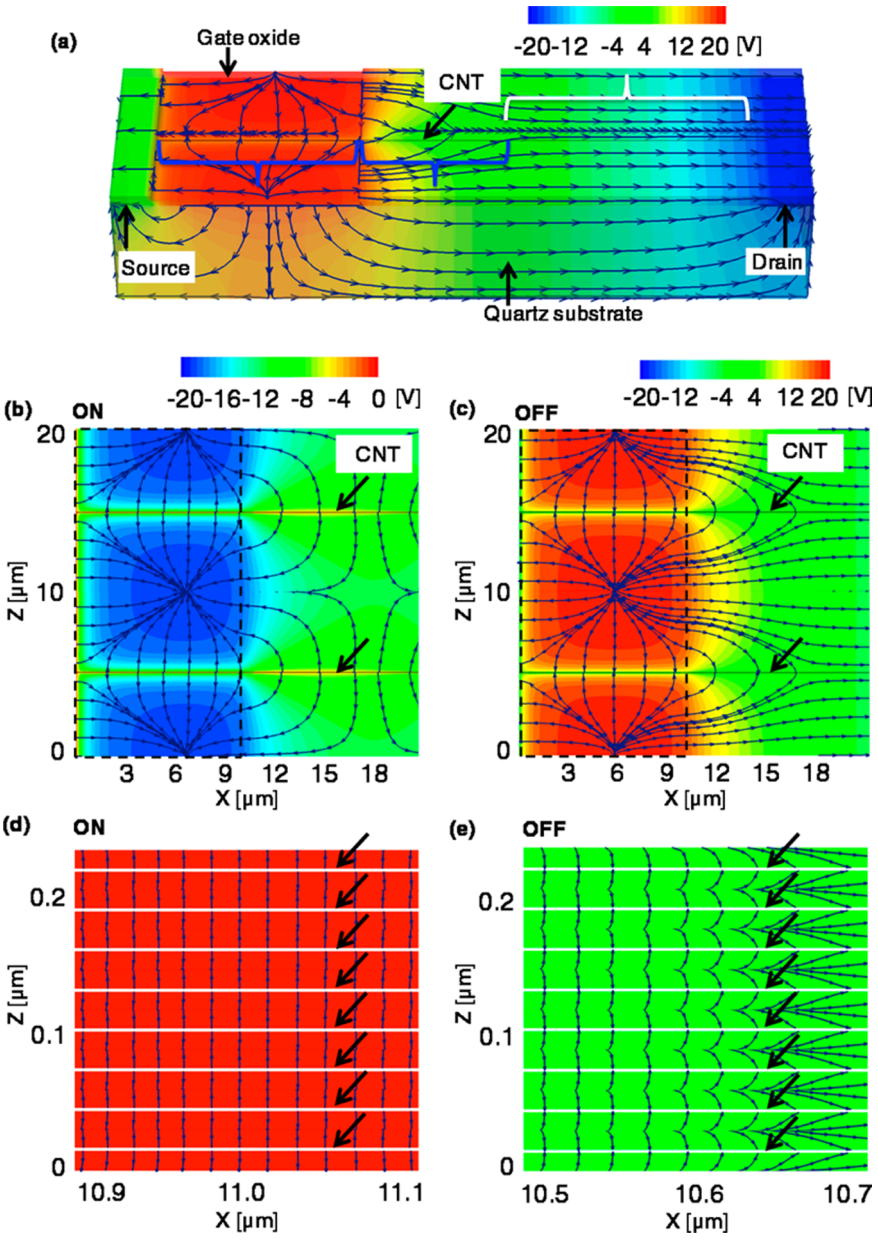

Figure 3. (a) Three-dimensional electric field lines (tangential to the surface) for PG-FET having $N = 0.1$ CNTs/μm in the OFF state. The left blue bracket covering the 10 μm gate length, together with the right blue, shows the region where electric field lines from the wings of the gate are terminating in the nanotube. Electric field lines under the white bracket prefer to terminate in the drain. (b,c) *XZ* cuts through the array of CNTs in the PG-FET of panel a for ON and OFF states. (d,e) Similar *XZ* cuts for PG-FET having $N = 33$ CNTs/μm.

$\sim 4.25 \times 10^{-8}$ A, that is, 24.4 μA/μm (see Figure 2b). This numerical result is within a factor of 2 of the current density obtained from a simple 2D charge-sheet calculation based on $I_{DS}/N = 1/2\mu_{avg}(\varepsilon_0\varepsilon_{OX}/T_{OX})(d/L)(V_{GS} - V_T)^2$, suggesting the validity of our numerical simulation. The profiles of the conduction band (Figure 2c) in the ON state under the gate show higher pull-up (stronger channel inversion) of the barrier for smaller N and result in higher I_{ON}. Figure 2e shows that thermionic (TH) injection of carriers over the hole-energy barrier near the source contact (injected carriers drift through the CNT) is the dominant current component in the ON state.

The OFF current (I_{DS} at $V_{GS} = 20$ V) per CNT (I_{OFF}/N) has V-shaped turn-around (Figure 2b): it first decreases as $I_{OFF}/N \sim N^{-1}$ for $N = 0.067-10$ CNTs/μm and then increases as $I_{OFF}/N \sim N^3$, for $N = 10-100$ CNTs/μm. The remarkable feature of I_{OFF} is unexpected from classical 2D electrostatics that would suggest a monotonous decrease in I_{OFF} with N (like the I_{ON} *vs* N relationship discussed above). The conduction band diagram shown in Figure 2d offers a clue regarding this nonintuitive V-shaped turn-around of I_{OFF} as a function of N. For same L_{OV}, PG-FET with $N \sim 100$ CNTs/μm has a rapid potential drop near the beginning of underlap region—analogous to the thin-film limit related to 2D

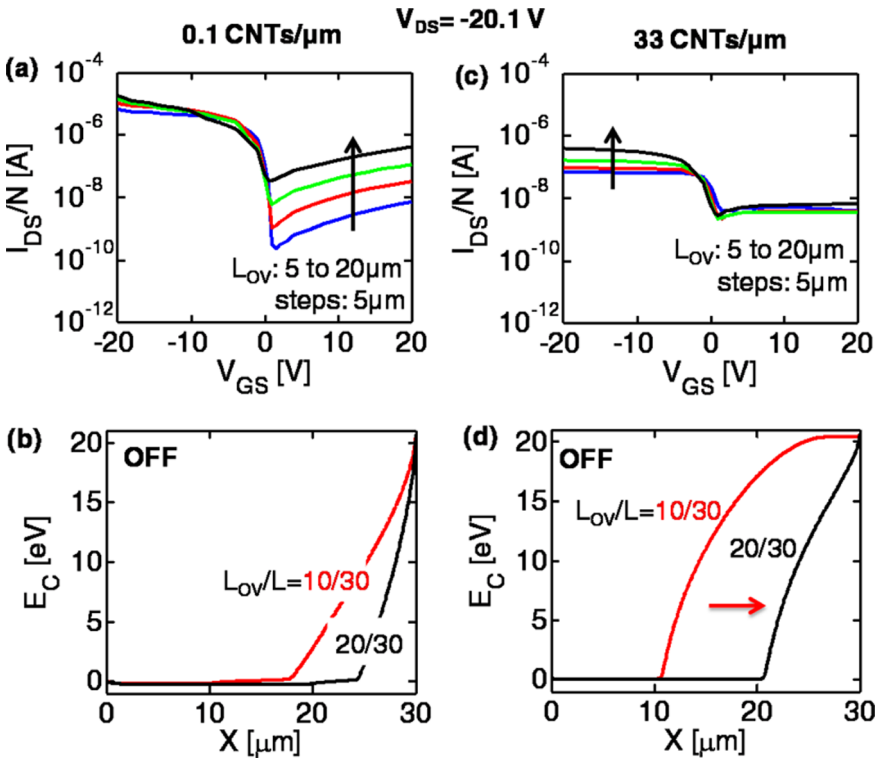

Figure 4. Simulated $I_{DS}-V_{GS}$ characteristics for different L_{OV} in PG-FETs with (a) N = 0.1 CNTs/μm, (c) N = 33 CNTs/μm. Conduction band profiles for different L_{OV} in the OFF state of PG-FETs with (b) N = 0.1 CNTs/μm, (d) N = 33 CNTs/μm.

electrostatics.[44,45] Resultant high electric field (>40 kV/cm) in that region induces high BTBT (Figure 2f) and hence large I_{OFF}. As N is decreased, the gate parasitically controls CNTs in the underlap region and reduces band bending and electric field, and hence BTBT and I_{OFF} (Figure 2f). Beyond the inflection point at $N \sim 10$ CNTs/μm, parasitic effect reduces band bending near the beginning of the underlap region, but increases band bending (and electric field) near the drain contact. This leads to increase BTBT and, therefore, I_{OFF} (Figure 2f).

In order to understand the extent of parasitic gate coupling in the underlap region, we explore the field profiles in PG-FET as obtained from 3D simulation and comment on the dimensionality of CNTs in PG-FET configurations. Figure 3a plots the 3D electric field (tangential component to the surface) for a PG-FET with $N = 0.1$ CNTs/μm biased in the OFF state with $V_{GS} =$ 20 V and $V_{DS} = -20.1$ V. The field lines originate at the gate and terminate at the CNT and at the source and drain contacts. The crucial role of finite density of states for a 1D CNT is obvious from the field profile: the field lines from the 3D gate and drain must travel along the channel through the quartz substrate before they can terminate onto the nanotube. Of the 3D field profile, a 2D cut in the XZ plane through the CNT highlights the salient features. Figure 3b,c plots such a 2D cut of the field profile in ON and OFF states, respectively, for $N = 0.1$ CNTs/μm. Though the field line directions are opposite in ON and OFF states due to the opposite gate biases, the virtual extended gate length (the underlap region of CNT over which the gate has direct control) remains the same in both cases. The field lines from the gate control CNT are $\sim$8 μm in the underlap region for substantial decay of the field, while the rest of the gate field lines couple directly to the drain contact, thereby explaining the gradual drop of potential in the underlap region at the lower density limit in Figure 2d. This emergence of the virtual gate (beyond the geometric edge of the real gate) through parasitic coupling of the 2D gate to the 1D CNT creates the nontrivial variation in potential profile (and I_{OFF}/N) as a function of N in Figure 2. The field lines from the gate of a PG-FET with high density of CNTs ($N = 33$ CNTs/μm for Figure 3d,e) terminate within a very short distance ($\sim$0.7$-$1 μm) in the underlap region, while the rest of the underlap region is controlled by the drain as an equipotential region. Such equipotential region in the underlap results from the p-type doping of CNTs due to interface defects; this region behaves like an implicit drain contact and explains the characteristic shape of potential drop along the CNT in Figure 2d.

The extents of parasitic gate control in PG-FETs with low- and high-density CNTs are also evident when L_{OV} is varied, while keeping L and T_{OX} fixed. For PG-FET with $N \sim 0.1$ CNTs/μm, an increase in L_{OV} increases I_{OFF} by orders of magnitude, while keeping the variation in I_{ON} relatively small (Figure 4a). Higher L_{OV} brings a larger part of the CNT under gate control and causes linear

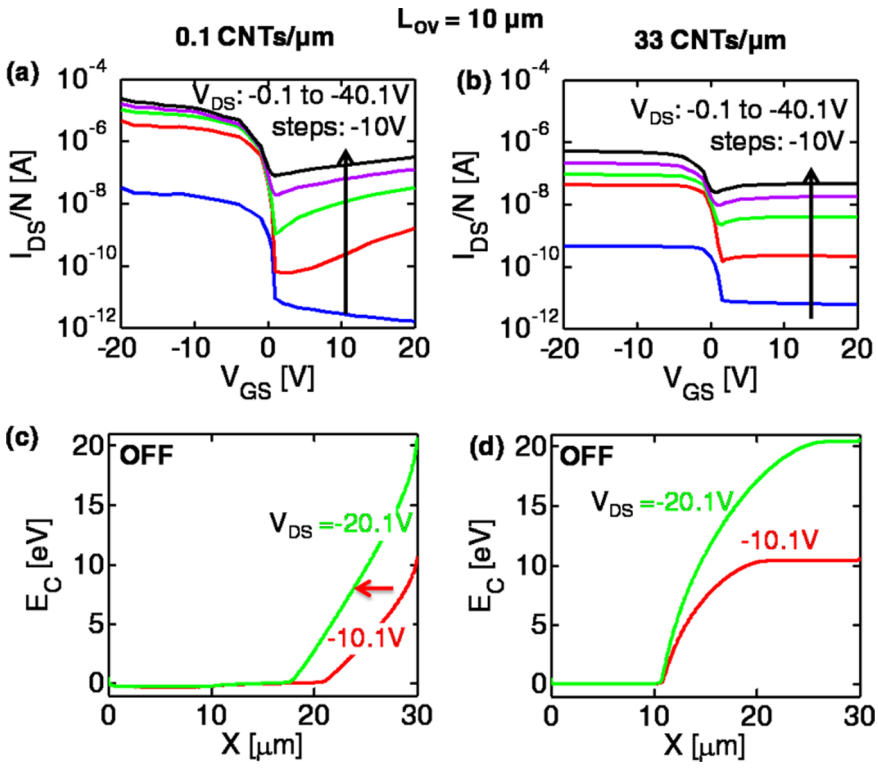

Figure 5. Simulated $I_{DS}-V_{GS}$ characteristics for different V_{DS} in PG-FETs with (a) N = 0.1 CNTs/μm, (b) N = 33 CNTs/μm. Conduction band profiles for different V_{DS} in the OFF state of PG-FETs with (c) N = 0.1 CNTs/μm, (d) N = 33 CNTs/μm.

increase in I_{ON} with L_{OV}. Exponential increase in I_{OFF} with L_{OV} arises from the increase in band bending (*i.e.*, electric field) in the underlap region near the drain (Figure 4b). Since the BTBT component of I_{OFF} depends exponentially on the electric field, a linear increase in electric field with L_{OV} causes exponential increase in I_{OFF}. On the other hand, for PG-FET with N = 33 CNTs/μm, parasitic gate control is less prominent and consequently the effect of L_{OV} variation is less dramatic (Figure 4c). The only increase in I_{ON} with L_{OV} results from the increase in electrostatic control in a greater portion of the CNT. Electric field (≡derivative of band profiles in Figure 4d) in the underlap region with variation in L_{OV}, however, remains essentially similar; therefore, the I_{OFF} is unchanged.

We finally discuss the extent of parasitic gate control as a function of drain bias for PG-FETs having different CNT densities. Figure 5a (for N = 0.1 CNTs/μm) and 5b (for N = 33 CNTs/μm) show higher increase in I_{ON}/N as V_{DS} changes from −0.1 to −10.1 V compared to the increase in I_{ON}/N for $V_{DS} < -10.1$ V. The presence of hole fluxes both in the drain and in the source sides at smaller $|V_{DS}|$ and the disappearance of the ones in the drain side at larger $|V_{DS}|$ are the reasons for such I_{ON}/N variation. I_{OFF}, on the other hand, is controlled by electric field in the underlap region primarily through BTBT (Figure 2f); therefore, I_{OFF} increases exponentially with $|V_{DS}|$ due to the increase in band bending (Figure 5c,d).

Experimental Validation. The three key theoretical predictions of parasitic gate coupling (*i.e.*, L_{OV} dependence of I_{OFF}/N in Figure 4, V_{DS} dependence of I_{ON}/N in Figure 5, and high OFF currents in Figure 5) in PG-FETs with low CNT density are explored using a series of experiments on PG-FETs with a single semiconducting CNT as the channel material. The low-density limit offers the most stringent test of the predictions of the model because the parasitic 3D-to-1D coupling is most pronounced for low tube densities.

Fabrication of such PG-FET (Schematic in Figure 6a) starts with the deposition of parallel stripes of iron (0.6 nm) as the catalyst on ST-cut quartz substrates, followed by CVD growth of single-wall aligned-array low-density (0.1−0.2 CNTs/μm) CNTs.[4,46] After photolithographic definition of source and drain electrodes (with $L \sim 30$ μm separation) *via* e-beam evaporation (Ti/Pd (2 nm/40 nm)) and lift-off, CNTs except those in narrow strips (~3 μm width) are completely removed by reactive ion etching (RIE). Single CNT devices are screened *via* SEM (and/or AFM) among devices with small numbers of CNTs, and the diameter of the CNT in the channel is determined by the analysis of Raman spectroscopy. After triple layers of gate dielectric (SOG/Al_2O_3/cross-linked PVA with effective oxide thickness (EOT) of 400 nm) are deposited on CNTs, Ti gate metal (50 nm) is photolithographically defined with a gate overlap L_{OV} = 5 μm by e-beam evaporation and lift-off. Finally, CNTs with semiconducting properties are confirmed by electrical measurements. After all electrical measurements for different V_{DS} are completed in vacuum (pressure = 1 × 10^{-4} Torr and temperature = 60 °C) in

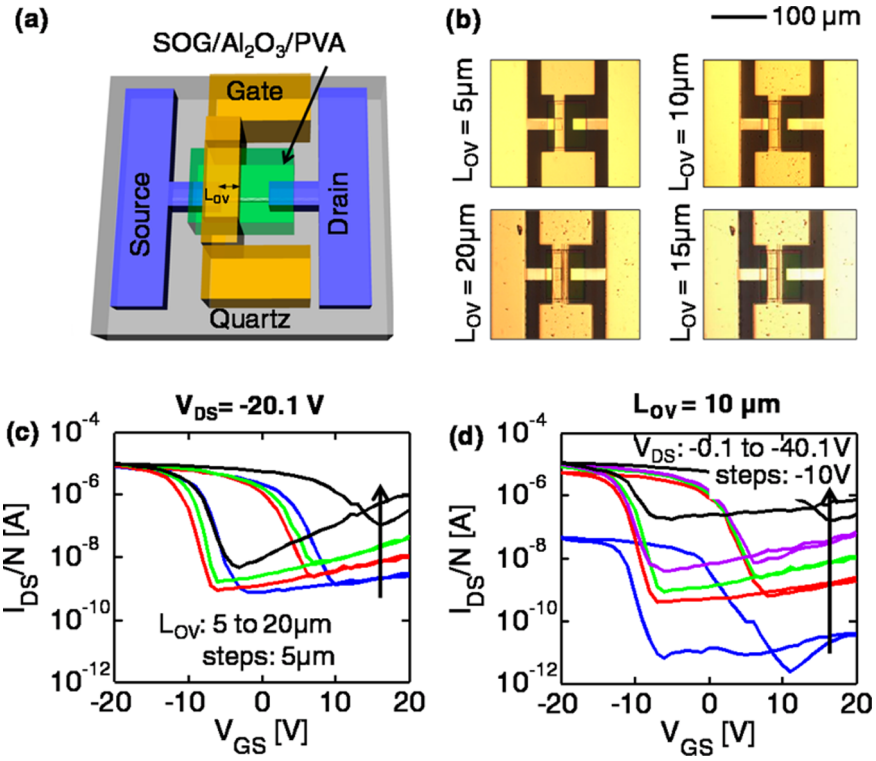

Figure 6. (a) Schematic of experimental structure of partial-gate CNTFET (PG-FET) with single semiconducting CNT (corresponding to $N \leq 0.1$ CNTs/μm limit) as the channel, (b) optical images for PG-FET with gradually increasing gate overlap from 5 to 20 μm. Experimental $I_{DS}-V_{GS}$ characteristics in PG-FETs with $N = 0.1$ CNTs/μm for (c) $V_{DS} = -20.1$ V, (d) $L_{OV} = 10$ μm.

order to avoid electrical breakdown of the CNT,[47] gate overlap (L_{OV}) for the same CNT PG-FET is extended *via* the same method above, followed by the same electrical characterization for each L_{OV} condition (Figure 6b shows optical micrograph of a PG-FET with different L_{OV}). In the experimental structure, the source, drain, and gate contact widths are such that we can assume $W_{G,S,D} \sim 30$ μm. Indeed for $W_{G,S,D} > 10$ μm, devices show negligible width dependency and currents, I_{DS}/N, saturate (Figure 2b). In this study, the diameter of the semiconducting CNT is estimated as $d \sim 1.67$ nm from G-band Raman spectra (Supporting Information Figure 2), and the illustration of the experimental procedures is provided through the schematic diagram in Supporting Information Figure 5.

Figure 6c plots the measured $I_{DS}-V_{GS}$ characteristics during a $V_{GS} = -20$ to 20 V sweep for PG-FETs with different L_{OV} at fixed V_{DS}, while Figure 6d plots the same measured at different V_{DS} with fixed L_{OV}. Measurements are remarkably similar to the simulation results obtained for PG-FETs with low-density CNTs (Figures 4a and 5a). ($N \sim 0.1$ CNTs/μm is a good approximation to simulate single CNT PG-FET, as the current for $N < 0.1$ CNTs/μm saturates in Figure 2b.) The only differences in terms of higher threshold voltage and larger subthreshold slope in the experiment reflect the omission of trapping–detrapping dynamics of interface and bulk defects[29] during simulation.

The synopsis of the key features (I_{ON}, I_{OFF}, and I_{ON}/I_{OFF}) of measured $I_{DS}-V_{GS}$ characteristics is provided in Figure 7 for PG-FETs fabricated with various levels of L_{OV}. At fixed L_{OV}, an increase in V_{DS} increases both I_{ON} (Figure 7a) and I_{OFF} (Figure 7b) because of the increase in the electric field along the CNT. Variation in L_{OV} also produces expected linear variation in I_{ON} (Figure 7a) and exponential variation in I_{OFF} (Figure 7b) and, therefore, a decrease in I_{ON}/I_{OFF} at higher V_{DS} and higher L_{OV} (Figure 7c), as expected for PG-FETs with large contact widths. Simulation of PG-FET based on the model discussed above confirms the experimental trend.

Parametric Dependence of Electrostatic Coupling. The remarkably complex interplay between the 3D electric field and the 1D CNT discussed above cannot be described by simplified numerical or analytical models. To check for the universality/robustness of our results, we vary gate oxide thickness (T_{OX}) and dielectric constant (ε_{OX}) and CNT diameter (d), and the results are summarized in Supporting Information Figures 6–11 and Supporting section 2. Although the $I_{DS}-V_{GS}$ characteristics change slightly as a function of device parameters, as long as a reasonably thick dielectric (such as quartz) is used as substrate for the CNT device, our results demonstrate that the gate channel parasitic coupling remains an important concern. This 3D capacitive coupling can be suppressed by using full-gate covering the entire channel. Even for partial gates, the coupling can be reduced by decreasing the gate width; see Supporting Information Figures 12 and 13. The gradual suppression of parasitic lines is obvious, especially at

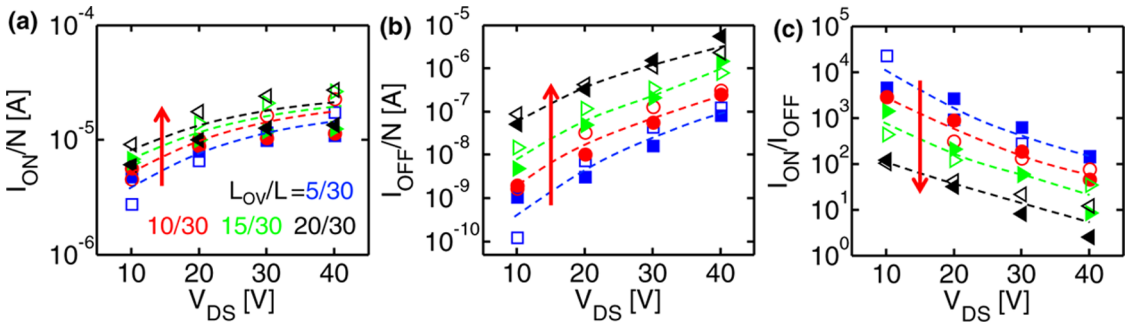

Figure 7. Simulated (open symbol) and experimental (solid symbol) (a) I_{ON}/N (at $V_{GS} = -20$ V) *vs* V_{DS}, (b) I_{OFF}/N (at $V_{GS} = 20$ V) *vs* V_{DS}, and (c) I_{ON}/I_{OFF} *vs* V_{DS}, as obtained from Figures 4–6.

0.1 μm gate width, because the parasitic field lines originating at the wings of the wider gate are now absent. This offers us an opportunity to work with partial-gated test structures whose results can be interpreted by simple classical models uncorrupted by fringing effects.

CONCLUSION

In summary, we have used a three-dimensional self-consistent model for partial-gate CNTFETs to demonstrate a surprisingly complex electrostatic interaction between 3D electric field and 1D NTs/NWs. Our results show the following results. (1) The parasitic coupling is most significant at low NT/NW densities, especially in the limit of electrostatically doped, single NT/NW devices. (2) Although the coupling is suppressed with increasing NT/NW densities, a V-shaped turn-around in the OFF current (Figure 2b) reflects the importance of 3D electrostatic coupling even at moderate NT/NW densities. (3) Since the substrate always offers a pathway for the 3D gate fields to terminate onto the 1D channel (Figure 1b) therefore, the parasitic coupling persists despite scaling of gate oxide thickness, increase in dielectric constant, and reduction of diameter of the NTs/NWs. (4) The OFF current is dominated by BTBT tunneling. At low NT/NW densities, I_{OFF} depends exponentially on overlap length, suggesting the importance of parasitic coupling. (5) The asymptotic charge-sheet limit is reached for partial gate devices at relatively high densities (>100 CNTs/μm).

The complexity of electrostatic interaction suggests a careful reconsideration of carrier transport in electrostatically doped diodes, tunnel FET, various other characterization/test structures, *etc.*, widely used for parameter extraction and technology development of CNT-based nano- and optoelectronics.

METHODS

Modeling Details. The simulation model for PG-FET self-consistently solves the electrostatics and charge density. To model electrostatics potential with the effect of contact dimension, we solve 3D Poisson equation

$$\nabla(\varepsilon\nabla V) = -\rho \quad (1)$$

Here, V is the spatial-dependent electrostatics potential and ε is the material-dependent permittivity. Charge density is $\rho = q(p - n - N_a^-)$, where q is the electron charge. Poisson equation is linked with continuity and drift-diffusion through hole and electron concentrations, p and n. The effect of negatively charged interfacial trap,[40,41] because of the inevitable presence of oxygen and water molecules on the surface of the CNTs, is represented through ionized impurity concentration N_a^-.

To obtain charge density, the following continuity equations are solved:

$$\frac{1}{q}\frac{dI_n}{dx} - R + G_{BBT,n} + G_{II,n} + G_{SBT,n} = 0; \frac{1}{q}\frac{dI_p}{dx} + R - G_{BBT,p} - G_{II,p} - G_{SBT,p} = 0 \quad (2)$$

where $R = \beta(np - n_i^2)$ is the radiative rate for direct band-to-band recombination,[35,48,49] β is the recombination coefficient, and n_i is the intrinsic carrier concentration of the CNT. Band-to-band tunneling, impact ionization, and Schottky barrier tunneling are represented as the generation in the CNT channel through the terms $G_{BTBT,n(p)}$, $G_{II,n(p)}$, and $G_{SBT,n(p)}$, respectively, for electron (hole). The expressions for $G_{BTBT,n(p)}$,[17,20,42,50] $G_{II,n(p)}$,[42] and $G_{SBT,n(p)}$,[35,51,52] along the channel region are

$$G_{BTBT,n(p)}(x) = \frac{5}{9}\frac{|dV/dx|^2 td}{\pi\hbar^2 v_F}\exp\left[-\frac{E_G^2}{\delta\hbar v_F|dV/dx|}\right] \quad (3)$$

$$G_{II,n(p)}(x) = \frac{5\times10^3 I_S}{q}\exp\left[-\frac{3E_G}{23.33|dV/dx|d}\right] \quad (4)$$

$$G_{SBT,n(p)} = \frac{\pi\left|\frac{dV}{dx}\right|ATtd}{k_B}\left[\exp\left[-\frac{2\sqrt{2m}}{\hbar}\int_0^x\sqrt{E_{rx,C(V)}}dr\right]\ln\left[\frac{1+\exp\eta_{n(p)}}{1+\exp\eta_{n(p),S}}\right] + \exp\left[-\frac{2\sqrt{2m}}{\hbar}\int_x^L\sqrt{E_{rx,C(V)}}dr\right]\ln\left[\frac{1+\exp\eta_{n(p)}}{1+\exp\eta_{n(p),D}}\right]\right] \quad (5)$$

Here, $\hbar$ is the reduced Planck's constant, t is the wall thickness of the CNT, and $|dV/dx|$ is the electric field along the channel direction. The Fermi velocity ($v_F \sim 10^8$ cm/s) is a characteristic of the band structure of the SWNTs.[17] The band gap of CNTs is related to the diameter of the tubes, $E_G = 0.7/d$ eV,[20] so that BTBT generation is more pronounced in larger diameter CNTs, as expected. The ideality factor, $\delta \sim 8.34$, within

the exponential function in eq 3 is used to match the theoretical results to the experiments (Figure 4 in the Supporting Information). It is noticeable that a simple analytical model uses a somewhat lower value of $\delta \sim 2.78$.[20,42] From eq 5, $\eta_{n,S(D)} = (E_{F,S(D)} - E_C)/k_BT$, $\eta_{p,S(D)} = (E_V - E_{F,S(D)})/k_BT$, $E_{rx,C} = E_C(r) - E_C(x)$, $E_{rx,V} = E_V(x) - E_V(r)$, and r is a position variable along the channel. Effective mass of electron and hole is $m = E_G m_0/20$, where m_0 is the mass of free carrier, $E_{F,S(D)}$ is the Fermi energy for carriers in S(D) contact, $A = 1.5 \times 10^2\ E_G A/cm^2/K^2$ is the Richardson constant, k_B is the Boltzmann constant, and T is the lattice temperature.

The I_S used in the prefactor of the impact ionization generation is the summation of all other current components (flow of the carriers may induce impact ionization depending on band bending magnitude and direction). In order for band-to-band tunneling to take place, the band potential must bend above E_G/q. The drift-diffusion current for electron (hole) $I_{n(p)}$ in eq 2 is represented as

$$I_n = -qn\mu_{FE}\frac{dV}{dx} + qD_n\frac{dn}{dx};\quad I_p = -qp\mu_{FE}\frac{dV}{dx} - qD_p\frac{dp}{dx} \qquad (6)$$

Here, the field-dependent mobility μ_{FE} is a function of CNT diameter,[25,35,36] and $D_{n(p)}$ is the diffusion coefficient of the electron (hole). The expressions μ_{FE} and $D_{n(p)}$ are provided in Supporting Information. Supporting Information Figure 3 sketches out the flow chart for simulation. The simulation procedures are explained in detail in the Supporting Information section 1.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Measurement and simulation procedures for 3D-CNTFETs. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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